

## Chapter 14: Semiconductor Electronics: Materials, Devices and Simple Circuits

### Example:

**Example 14.1:** C, Si and Ge have same lattice structure. Why is C insulator while Si and Ge intrinsic semiconductors?

**Solution:** The four bonding electrons of C, Si, or Ge are located in the second, third, and fourth orbits, respectively. As a result, the energy required to extract an electron from these atoms (ionisation energy  $E_g$ ) will be lowest for Ge, highest for Si, and lowest for C. As a result, while the number of free electrons for conduction in Ge and Si is large, it is negligible in C.

**Example 14.2:** Suppose a pure Si crystal has  $5 \times 10^{28}$  atoms  $m^{-3}$ . It is doped by 1 ppm concentration of pentavalent As. Calculate the number of electrons and holes. Given that  $n_i = 1.5 \times 10^{16} m^{-3}$ .

**Solution:** When compared to doped electrons  $n_i = 1.5 \times 10^{16} m^{-3}$ , thermally generated electrons ( $n_i \sim 10^{16} m^{-3}$ ) are negligibly small as compared to those produced by doping. Therefore,  $n_e \approx ND$ . Since  $n_e n_h = n_i^2$ , The number of holes

$$\begin{aligned}
 n_h &= (2.25 \times 10^{32}) / (5 \times 10^{22}) \\
 &\sim 4.5 \times 10^9 m^{-3}
 \end{aligned}$$

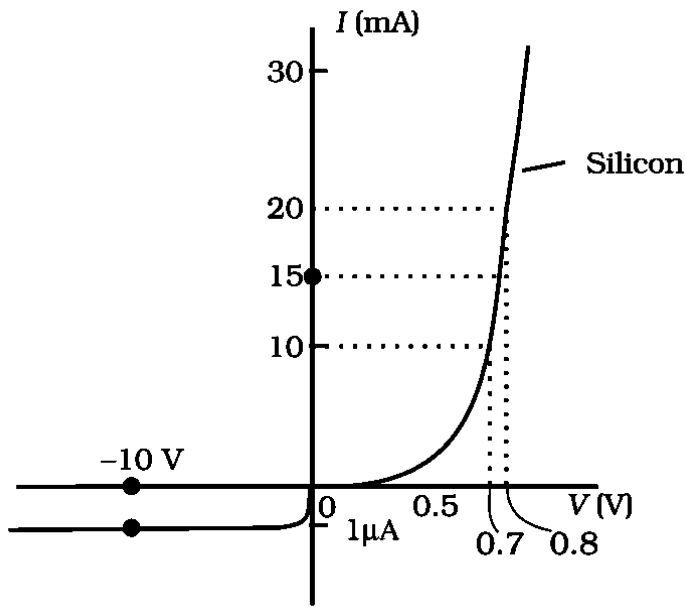
**Example 14.3:** Can we take one slab of p-type semiconductor and physically join it to another n-type semiconductor to get p-n junction?

**Solution:** No! Any slab, no matter how flat, will have roughness significantly larger than the inter-atomic crystal gap ( $\sim 2$  to  $3 \text{ \AA}$ ), making continuous atomic contact impossible. For the flowing charge carriers, the junction will act as a discontinuity.

**Example 14.4:** The V-I characteristic of a silicon diode is shown in the Fig. 14.17. Calculate the resistance of the diode at

(a)  $I_D = 15 \text{ mA}$

(b)  $V_D = -10 \text{ V}$



**Solution:** Using Ohm's law, we may compute the resistance by considering the diode characteristics as a straight line flowing through the origin.

$I = 10 \text{ mA}$  to  $I = 20 \text{ mA}$  w.

(a) From the curve, at

$I = 20 \text{ mA}, V = 0.8 \text{ V}; I = 10 \text{ mA}, V = 0.7 \text{ V}$

$$\begin{aligned}
 r_{fb} &= \frac{\Delta V}{\Delta I} \\
 &= \frac{0.1 \text{ V}}{10 \text{ mA}} \\
 &= 10 \Omega
 \end{aligned}$$

(b) From the curve at,

$V = -10 \text{ V}, I = -1 \mu\text{A}$ ,

Therefore,

$$\begin{aligned}
 r_{rb} &= \frac{10 \text{ V}}{1 \mu\text{A}} \\
 &= 1.0 \times 10^7 \Omega
 \end{aligned}$$

**Example 14.5:** In a Zener regulated power supply a Zener diode with  $V_z = 6.0 \text{ V}$  is used for regulation. The load current is to be  $4.0 \text{ mA}$  and the unregulated input is  $10.0 \text{ V}$ . What should be the value of series resistor  $R_S$ ?

**Solution:** The value of  $R_S$  should be such that the current flowing through the Zener diode is much greater than the current flowing through the load. This is necessary for proper load management.

Decide on a Zener current that is five times the load current, i.e.  $I_z = 20 \text{ mA}$ . As a result, the total current via RS is. Across RS, there is a voltage drop of  $10.0 - 6.0 = 4.0 \text{ V}$

This results in  $RS = 4.0\text{V} / (24 \times 10^{-3})\text{A} = 167 \Omega$ . The carbon resistor's closest value is  $150 \Omega$ .

As a result, a series resistor of is suitable. It's worth noting that minor variations in the resistor's value are unimportant; what matters is that the current  $I_z$  is significantly larger than  $I_L$ .

**Example 14.6:** The current in the forward bias is known to be more ( $\sim \text{mA}$ ) than the current in the reverse bias ( $\sim \mu\text{A}$ ). What is the reason then to operate the photodiodes in reverse bias?

**Solution:** Take, for example, an n-type semiconductor. The majority carrier density ( $n$ ) is obviously much higher than the minority hole density ( $p$ ). Let the excess electrons and holes generated by light be  $\Delta n$  and  $\Delta p$ , respectively:

$$n' = n + \Delta n$$

$$p' = p + \Delta p$$

Here are the electron and hole concentrations at any given illumination, while  $n$  and  $p$  are the carrier concentrations when no illumination is present.

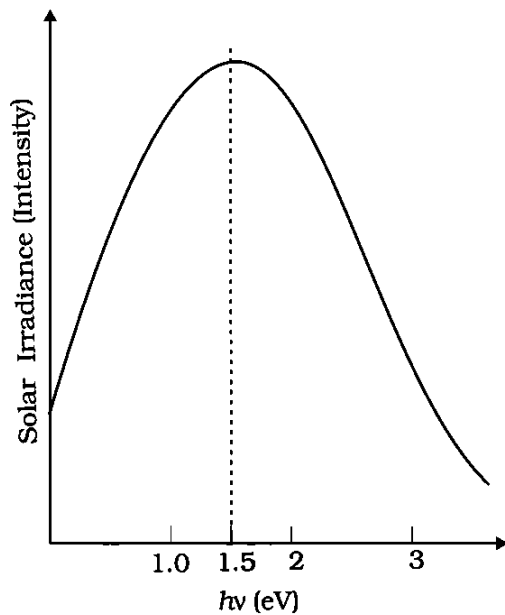
Keep in mind  $\Delta n = \Delta p$ ,  $n \gg p$ . As a result, the fractional change in majority carriers (i.e.  $\frac{\Delta n}{n}$ )

would be substantially smaller than in minority carriers (i.e.  $\frac{\Delta p}{p}$ ). In general, the fractional change in

the minority carrier dominated reverse bias current owing to photo-effects is easier to measure than the fractional change in the forward bias current. As a result, photodiodes are best employed to measure light intensity in reverse bias conditions.

**Example 14.7:** Why are Si and GaAs are preferred materials for solar cells?

**Solution:** The solar radiation spectrum received by us is shown in Figure.



The peaks are at  $1.5\text{eV}$ .  $h\nu > E_g$  for photo-excitation

Hence, a semiconductor having a band gap of  $1.5\text{eV}$  or less is more likely to perform well.

efficiency of solar conversion Silicon contains  $E_g$ .  $1.1\text{eV}$ , whereas GaAs has a value of  $1.1\text{eV}$ .

$1.53\text{eV}$  is the energy of a proton. In fact, GaAs is superior to GaAs (despite the

greater band gap). Si has a higher absorption coefficient than other elements. If we so desire,

CdS or CdSe materials (for example), We can only use the high voltage ( $2.4\text{eV}$ ).

photo-conversion energy component of solar energy and a large amount of energy will be wasted. The question arises as to why we do not use PbS (for example) as a material.

$\sim 0.4\text{eV}$ ) They satisfy the  $h\nu > E_g$  criterion for maxima that correspond to the

Spectra of solar radiation? If we do so, the majority of solar energy will be absorbed on the top layer of the solar cell and will not reach the depletion region or even close to it. Because of the junction field, we want photo-generation to occur only in the junction region for effective electron-hole separation.

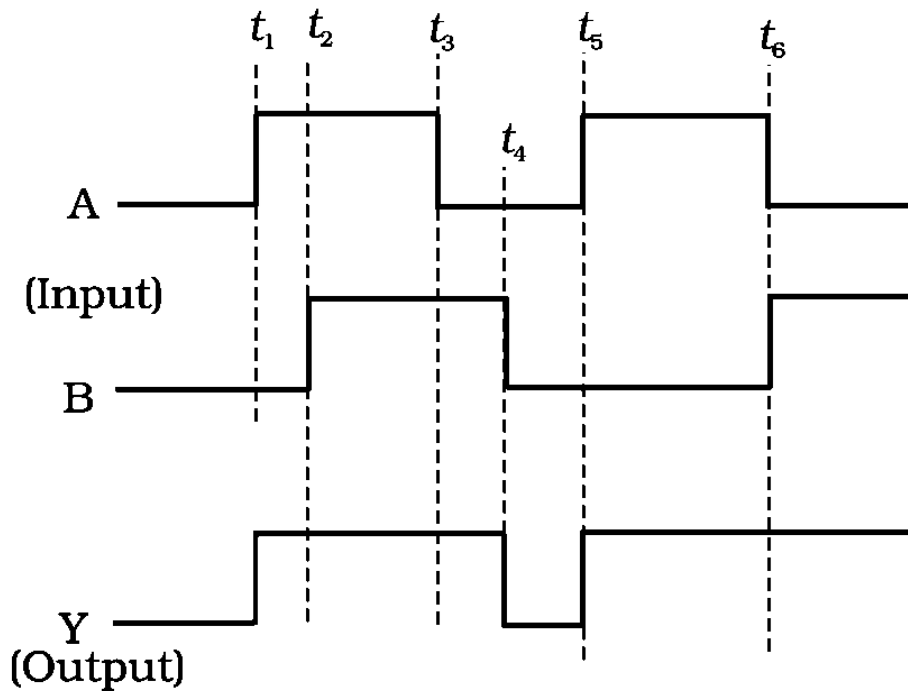
**Example 14.8:** Justify the output waveform (Y) of the OR gate for the following inputs A and B given in Fig. 14.30.

**Solution:** Note the following:

- At  $t < t_1$  :  $A = 0, B = 0$ ; Hence  $Y = 0$
- For  $t_1$  to  $t_2$  :  $A = 1, B = 0$ ; Hence  $Y = 1$
- For  $t_2$  to  $t_3$ ;  $A = 1, B = 1$ ; Hence  $Y = 1$
- For  $t_3$  to  $t_4$ ;  $A = 0, B = 1$ ; Hence  $Y = 1$

- For  $t_4$  to  $t_5$ :  $A = 0, B = 0$ ; Hence  $Y = 0$
- For  $t_5$  to  $t_6$ ;  $A = 1, B = 0$ ; Hence  $Y = 1$
- For  $t > t_6$ ;  $A = 0, B = 1$ ; Hence  $Y = 1$

Therefore the waveform  $Y$  will be as shown in the Fig. 14.30.

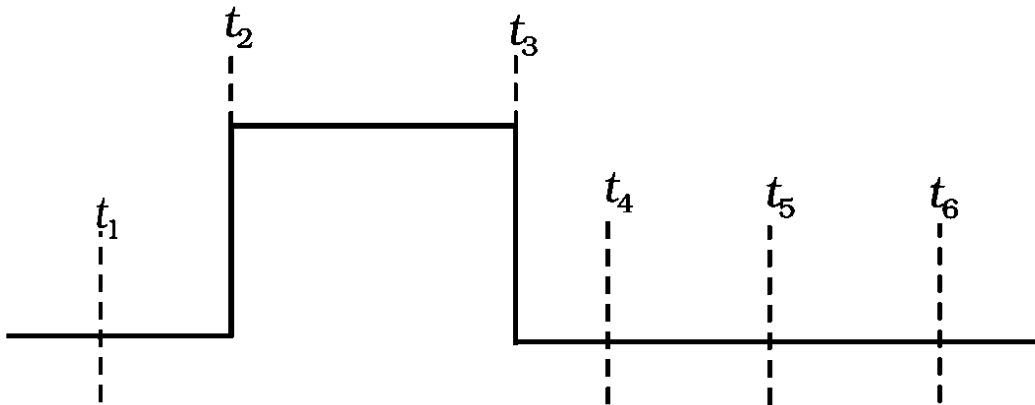


**Example 14.9:** Take A and B input waveforms similar to that in Example 14.8. Sketch the output waveform obtained from AND gate.

**Solution:**

- For  $t \leq t_1$ ;  $A = 0, B = 0$ ; Hence  $Y = 0$
- For  $t_1$  to  $t_2$ ;  $A = 1, B = 0$ ; Hence  $Y = 0$
- For  $t_2$  to  $t_3$ ;  $A = 1, B = 1$ ; Hence  $Y = 1$
- For  $t_3$  to  $t_4$ ;  $A = 0, B = 1$ ; Hence  $Y = 0$
- For  $t_4$  to  $t_5$ ;  $A = 0, B = 0$ ; Hence  $Y = 0$
- For  $t_5$  to  $t_6$ ;  $A = 1, B = 0$ ; Hence  $Y = 0$
- For  $t > t_6$ ;  $A = 0, B = 1$ ; Hence  $Y = 0$

Based on the above, the output waveform for AND gate can be drawn as shown below.

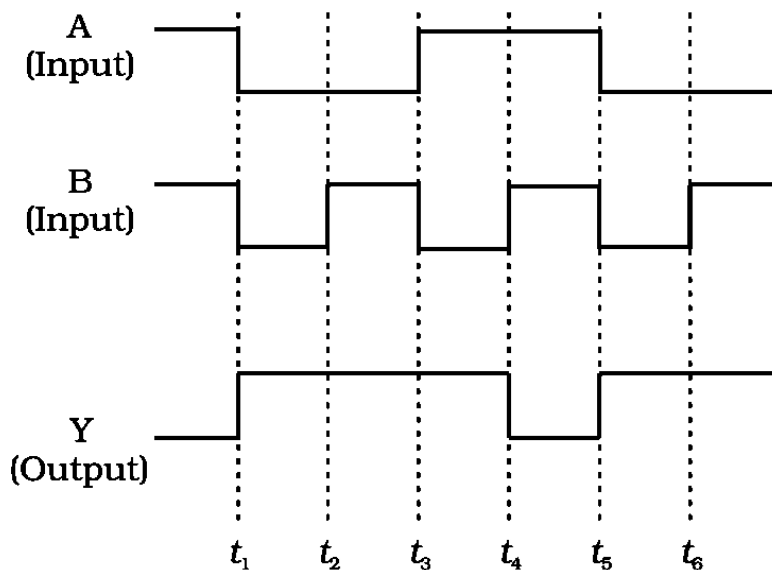


**Example 14.10:** Sketch the output  $Y$  from a NAND gate having inputs

$A$  and  $B$  given below:

**Solution:**

- For  $t < t_1$ ;
- For  $t_1$  to  $t_2$ ;  $A = 0, B = 0$ ; Hence  $Y = 1$
- For  $t_2$  to  $t_3$ ;  $A = 0, B = 1$ ; Hence  $Y = 1$
- For  $t_3$  to  $t_4$ ;  $A = 1, B = 0$ ; Hence  $Y = 1$
- For  $t_4$  to  $t_5$ ;  $A = 1, B = 1$ ; Hence  $Y = 0$
- For  $t_5$  to  $t_6$ ;  $A = 0, B = 0$ ; Hence  $Y = 1$
- For  $t > t_6$ ;  $A = 0, B = 1$ ; Hence  $Y = 1$



## EXERCISES

**Question 14.1:** In an n-type silicon, which of the following statement is true:

- (a) Electrons are majority carriers and trivalent atoms are the dopants.
- (b) Electrons are minority carriers and pentavalent atoms are the dopants.
- (c) Holes are minority carriers and pentavalent atoms are the dopants.
- (d) Holes are majority carriers and trivalent atoms are the dopants.

**Solution:** The correct statement is (c).

The electrons are the majority carriers in n-type silicon, whereas the holes are the minority carriers. When pentavalent elements, such as phosphorus, are doped in silicon atoms, an n-type semiconductor is formed.

**Question 14.2:** Which of the statements given in Exercise 14.1 is true for p-type semiconductors.

**Solution:** The correct statement is (d)

The holes are the majority carriers in a p-type semiconductor, whereas the electrons are the minority carriers. When trivalent elements, such as aluminium, are doped in silicon atoms, a p-type semiconductor is formed.

**Question 14.3:** Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to  $(E_g)_C$ ,  $(E_g)_{Si}$  and  $(E_g)_{Ge}$ . Which of the following statements is true?

- (a)  $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$
- (b)  $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$
- (c)  $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$
- (d)  $(Eg)_C = (Eg)_{Si} = (Eg)_{Ge}$

**Solution:** The correct statement is (c)

Carbon has the largest energy band gap of the three elements, while germanium has the smallest.

These elements' energy band gaps are related as follows:  $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$

**Question 14.4:** In an unbiased p-n junction, holes diffuse from the p-region to n-region because

- (a) free electrons in the n-region attract them.
- (b) they move across the junction by the potential difference.
- (c) hole concentration in p-region is more as compared to n-region.
- (d) All the above.

**Solution:** The correct statement is (c)

Charge carriers diffuse across a junction from a region of higher concentration to a region of lower concentration. The p-region has a higher concentration of holes than the n-region in this situation. As a result, holes diffuse from the p-region to the n-region in an unbiased p-n junction.

**Question 14.5:** When a forward bias is applied to a p-n junction, it

- (a) raises the potential barrier.
- (b) reduces the majority carrier current to zero.
- (c) lowers the potential barrier.
- (d) None of the above.

**Solution:** The correct statement is (c)

When a forward bias is applied to a p-n junction, the potential barrier is reduced. The potential barrier opposes the applied voltage in the case of a forward bias. As a result, the potential barrier at the intersection is minimised.

**Question 14.6:** For transistor action, which of the following statements are correct:

- (a) Base, emitter and collector regions should have similar size and doping concentrations.
- (b) The base region must be very thin and lightly doped.
- (c) The emitter junction is forward biased and collector junction is reverse biased.
- (d) Both the emitter junction as well as the collector junction are forward biased.

**Solution:** The correct statement is (b), (c).

The junction must be lightly doped for transistor action, with a very thin base area. In addition, the emitter and collector junctions must be forward-biased and reverse-biased, respectively.

**Question 14.7:** For a transistor amplifier, the voltage gain



- (a) remains constant for all frequencies.
- (b) is high at high and low frequencies and constant in the middle frequency range.
- (c) is low at high and low frequencies and constant at mid frequencies.
- (d) None of the above.

**Solution:** The correct statement is (c).

A transistor amplifier's voltage gain is constant only in the mid-frequency region. At both high and low frequencies, it is quite low.

**Question 14.8:** In half-wave rectification, what is the output frequency if the input frequency is 50Hz . What is the output frequency of a full-wave rectifier for the same input frequency.

**Solution:** Input frequency = 50 Hz

For a half-wave rectifier, the output frequency is equal to the input frequency.

∴ Output frequency = 50Hz

For a full-wave rectifier, the output frequency is twice the input frequency.

∴ Output frequency =  $2 \times 50 = 100\text{Hz}$

**Question 14.9:** For a CE-transistor amplifier, the audio signal voltage across the collected resistance of  $2\text{k}\Omega$  is  $2\text{V}$  . Suppose the current amplification factor of the transistor is 100 , find the input signal voltage and base current, if the base resistance is  $1\text{k}\Omega$  .

**Solution:** Collector resistance,  $R_c = 2\text{k}\Omega = 2000\Omega$

Audio signal voltage across the collector resistance,  $V = 2\text{V}$

Current amplification factor of the transistor,  $\beta = 100$

Base resistance,  $R_B = 1\text{k}\Omega = 1000\Omega$

Input signal voltage =  $V_i$

Base current =  $I_B$

We have the amplification relation as:

$$\text{Voltage amplification} = \frac{V}{V_i} = \beta \frac{R_C}{R_B}$$

$$\begin{aligned}
 V_i &= \frac{V R_B}{\beta R_C} \\
 &= \frac{2 \times 1000}{100 \times 2000} \\
 &= 0.01 \text{ V}
 \end{aligned}$$

Therefore, the input signal voltage of the amplifier is 0.01 V .

Base resistance is given by the relation:

$$\begin{aligned}
 R_B &= \frac{V_i}{I_B} \\
 &= \frac{0.01}{1000} \\
 &= 10 \times 10^{-6} \mu\text{A}
 \end{aligned}$$

**Question 14.10:**

Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 volt, calculate the output ac signal.

**Solution:** Voltage gain of the first amplifier,  $V_1 = 10$

Voltage gain of the second amplifier,  $V_2 = 20$

Input signal voltage,  $V_i = 0.01 \text{ V}$

Output AC signal voltage =  $V_o$ .

The total voltage gain of a two-stage cascaded amplifier is given by the product of voltage gains of both the stages, i.e.,

$$\begin{aligned}
 V &= V_1 \times V_2 \\
 &= 10 \times 20 \\
 &= 200
 \end{aligned}$$

We have the relation:

$$\begin{aligned}
 V &= \frac{V_o}{V_i} \\
 V_o &= V \times V_i \\
 &= 200 \times 0.01 \\
 &= 2 \text{ V}
 \end{aligned}$$

Therefore, the output AC signal of the given amplifier is 2 V .

**Question 14.11:** A p-n photodiode is fabricated from a semiconductor with band gap of 2.8eV . Can it detect a wavelength of 6000nm ?

**Solution:** Energy band gap of the given photodiode,  $E_g = 2.8\text{eV}$

Wavelength,  $\lambda = 6000 \text{ nm} = 6000 \times 10^{-9} \text{ m}$

The energy of a signal is given by the relation:

$$E = \frac{hc}{\lambda}$$

Where, h = Planck's

Constant =  $6.626 \times 10^{-34} \text{ Js}$

c = Speed of light

$$= 3 \times 10^8 \text{ m/s} = \frac{6.626 \times 10^{-34} \times 3 \times 10^8}{6000 \times 10^{-9}} = 3.313 \times 10^{-20} \text{ J}$$

$$\text{But } 1.6 \times 10^{-19} \text{ J} = 1\text{eV} \therefore E = 3.313 \times 10^{-20} \text{ J} = \frac{3.313 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.207\text{eV}$$

The energy of a signal of wavelength 6000nm is 0.207eV , which is less than 2.8eV the energy band gap of a photodiode. Hence, the photodiode cannot detect the signal.

**Question 14.12:** The number of silicon atoms per  $\text{m}^3$  is  $5 \times 10^{28}$  . This is doped simultaneously with  $5 \times 10^{22}$  atoms per  $\text{m}^3$  of Arsenic and  $5 \times 10^{20}$  per  $\text{m}^3$  atoms of Indium. Calculate the number of electrons and holes. Given that  $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$  . Is the material n-type or p-type?

**Solution:** Number of silicon atoms,  $N = 5 \times 10^{28} \text{ atoms /m}^3$

Number of arsenic atoms,  $n_{As} = 5 \times 10^{22} \text{ atoms /m}^3$

Number of indium atoms,  $n_{In} = 5 \times 10^{20} \text{ atoms /m}^3$

Number of thermally-generated electrons,  $n_i = 1.5 \times 10^{16} \text{ electrons /m}^3$

Number of electrons,  $n_e = 5 \times 10^{22} - 1.5 \times 10^{16} \approx 4.99 \times 10^{22}$

Number of holes =  $n_h$

In thermal equilibrium, the concentrations of electrons and holes in a semiconductor are related as:

$$n_e n_h = n_i^2$$

$$\begin{aligned} \therefore n_h &= \frac{n_i^2}{n_e} \\ &= \frac{(1.5 \times 10^{16})^2}{4.99 \times 10^{22}} \approx 4.51 \times 10^9 \end{aligned}$$

Therefore, the number of electrons is approximately  $4.99 \times 10^{22}$  and the number of holes is about  $4.51 \times 10^9$ . Because the number of electrons is more than the number of holes, the material is an n-type semiconductor.

**Question 14.13:** In an intrinsic semiconductor the energy gap  $E_g$  is  $1.2 \text{ eV}$ . Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at  $600 \text{ K}$  and that at  $300 \text{ K}$ ? Assume that the temperature dependence of intrinsic carrier

concentration  $n_i$  is given by  $n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$  where  $n_0$  is a constant.

**Solution:** Energy gap of the given intrinsic semiconductor,  $E_g = 1.2 \text{ eV}$

The temperature dependence of the intrinsic carrier-concentration is written as:

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

Where,  $k_B =$  Boltzmann constant  $= 8.62 \times$

$10^{-5} \text{ eV / KT} =$  Temperature  $n_0 =$  Constant

Initial temperature,  $T_1 = 300 \text{ K}$

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i1} = n_0 \exp\left[-\frac{E_g}{2k_B \times 300}\right] \dots(1)$$

Final temperature,  $T_2 = 600 \text{ K}$

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i2} = n_0 \exp\left[-\frac{E_g}{2k_B \times 600}\right] \dots(2)$$

The ratio between the conductivities at  $600 \text{ K}$  and at  $300 \text{ K}$  is equivalent to the ratio between the respective intrinsic carrier-concentrations at both temperatures.

$$\begin{aligned}
 \frac{n_{i2}}{n_{i1}} &= \frac{n_0 \exp\left[-\frac{E_g}{2k_B 600}\right]}{n_0 \exp\left[-\frac{E_g}{2k_B 300}\right]} \\
 &= \exp\frac{E_g}{2k_B} \left[ \frac{1}{300} - \frac{1}{600} \right] \\
 &= \exp\left[ \frac{1.2}{2 \times 8.62 \times 10^{-5}} \times \frac{2-1}{600} \right] \\
 &= \exp[11.6] = 1.09 \times 10^5
 \end{aligned}$$

Therefore, the ratio between the conductivities is  $1.09 \times 10^5$ .

**Question 14.14:** In a p-n junction diode, the current  $I$  can be expressed as

$I = I_0 \exp\left(\frac{eV}{2k_B T} - 1\right)$  where  $I_0$  is called the reverse saturation current,  $V$  is the voltage across the diode and is positive for forward bias and negative for reverse bias, and  $I$  is the current through the diode,  $k_B$  is the Boltzmann constant ( $8.6 \times 10^{-5} \text{ eV / K}$ ) and  $T$  is the absolute temperature. If for a given diode  $I_0 = 5 \times 10^{-12} \text{ A}$  and  $T = 300 \text{ K}$ , then

- What will be the forward current at a forward voltage of  $0.6 \text{ V}$  ?
- What will be the increase in the current if the voltage across the diode is increased to  $0.7 \text{ V}$  ?
- What is the dynamic resistance?
- What will be the current if reverse bias voltage changes from  $1 \text{ V}$  to  $2 \text{ V}$  ?

**Solution:** In a p-n junction diode, the expression for current is given as:

$$I = I_0 \exp\left(\frac{eV}{2k_a T} - 1\right)$$

Where,

$$I_0 = \text{Reverse saturation current} = 5 \times 10^{-12} \text{ A}$$

$$T = \text{Absolute temperature} = 300 \text{ K}$$

$$k_B = \text{Boltzmann constant} = 8.6 \times 10^{-5} \text{ eV / K} = 1.376 \times 10^{-23} \text{ J K}^{-1}$$

$V =$  Voltage across the diode

- Forward voltage,  $V = 0.6 \text{ V}$

$$\therefore \text{Current, } I = 5 \times 10^{-12} \left[ \exp \left( \frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300} \right) - 1 \right]$$

$$= 5 \times 10^{-12} \times \exp[22.36]$$

$$= 0.0256 \text{ A}$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage,  $V' = 0.7 \text{ V}$ , we can write:

$$I' = 5 \times 10^{-12} \left[ \exp \left( \frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} \right) - 1 \right]$$

$$= 5 \times 10^{-12} \times \exp[26.25]$$

$$= 1.257 \text{ A}$$

Hence, the increase in current,  $\Delta I = I' - I = 1.257 - 0.0256 = 1.23 \text{ A}$

$$(c) \text{ Dynamic resistance} = \frac{\text{Change in voltage}}{\text{Change in current}}$$

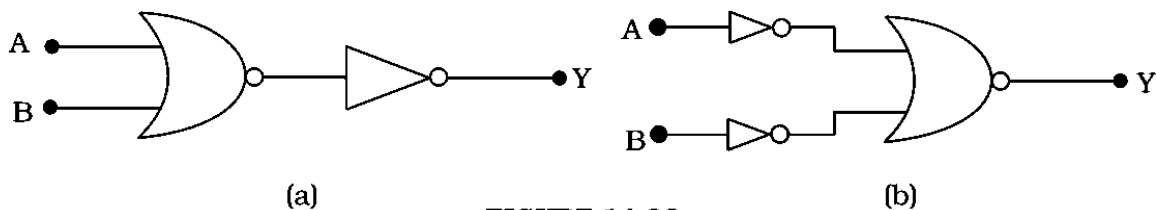
$$= \frac{0.7 - 0.6}{1.23}$$

$$= \frac{0.1}{1.23}$$

$$= 0.081 \Omega$$

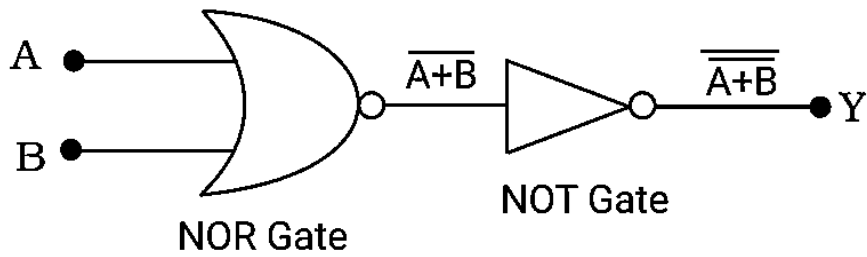
(d) If the reverse bias voltage changes from 1 V to 2 V, then the current ( $I$ ) will almost remain equal to  $I_0$  in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

**Question 14.15:** You are given the two circuits as shown in Fig. 14.36 Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



**FIGURE 14.36**

**Solution:** (a)  $A$  and  $B$  are the inputs and  $Y$  is the output of the given circuit. The left half of the given figure acts as the NOR Gate, while the right half acts as the NOT Gate. This is shown in the following figure.



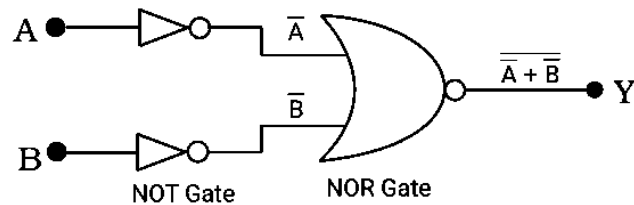
Hence, the output of the NOR Gate =  $\overline{A+B}$

This will be the input for the NOT Gate. Its output will be  $\overline{\overline{A+B}} = A+B$

$\therefore Y = A+B$

Hence, this circuit functions as an OR Gate.

(b)  $A$  and  $B$  are the inputs and  $Y$  is the output of the given circuit. It can be observed from the following figure that the inputs of the right half NOR Gate are the outputs of the two NOT Gates.

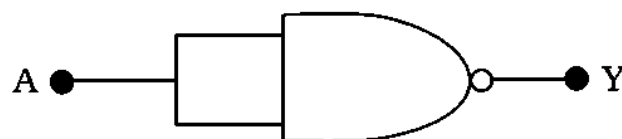


Hence, the output of the given circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

Hence, this circuit functions as an AND Gate.

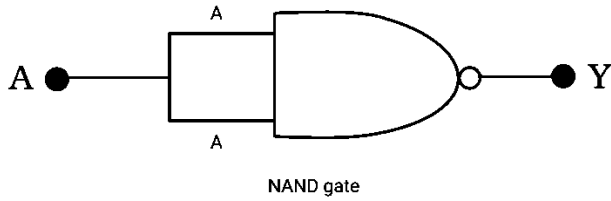
**Question 14.16:** Write the truth table for a NAND gate connected as given in Fig. 14.37.



**FIGURE 14.37**

Hence identify the exact logic operation carried out by this circuit.

**Solution:** A acts as the two inputs of the NAND gate and Y is the output, as shown in the following figure.



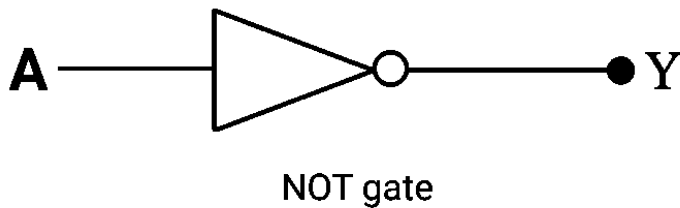
Hence, the output can be written as:

$$Y = \overline{A \cdot A} = \overline{A} + \overline{A} = \overline{A} \dots (1)$$

The truth table for equation (1) can be drawn as:

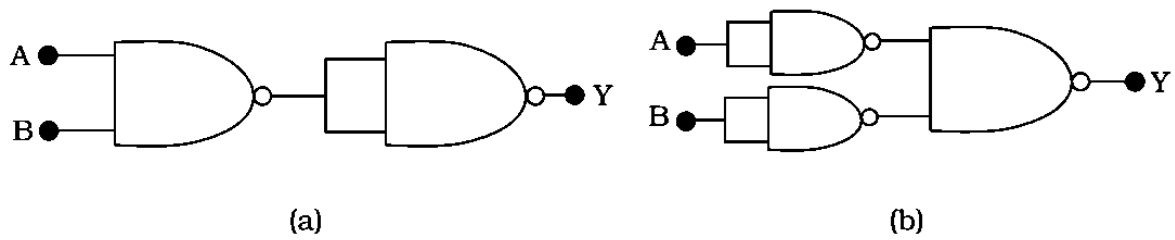
A	$Y = \overline{A}$
0	1
1	0

This circuit functions as a NOT gate. The symbol for this logic circuit is shown as:



**Question 14.17:** You are given two circuits as shown in Fig. 14.38, which consist of NAND gates. Identify the logic operation carried out by the two circuits.





**FIGURE 14.38**

**Solution:** In both the given circuits, A and B are the inputs and Y is the output.

(a) The output of the left NAND gate will be  $\overline{A \cdot B}$ .

Hence, the output of the combination of the two NAND gates is given as.

$$\begin{aligned}
 Y &= \overline{\overline{A \cdot B} \cdot \overline{A \cdot B}} \\
 &= \overline{\overline{A} \overline{B} + \overline{A} \overline{B}} \\
 &= AB
 \end{aligned}$$

Hence the circuit functions as an AND gate.

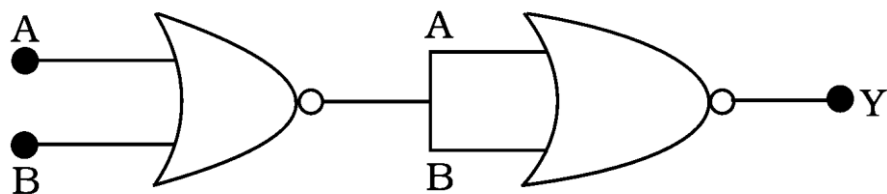
(b)  $\overline{A}$  is the output of the upper left of the NAND gate and  $\overline{B}$  is the output of the lower half of the NAND gate.

Hence, the output of the combination of the NAND gates will be given as:

$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

Hence, this circuit functions as an OR gate.

**Question 14.18:** Write the truth table for circuit given in Fig. 14.39 below consisting of NOR gates and identify the logic operation (OR, AND, NOR) which this circuit is performing.



**FIGURE 14.39**

(Hint:  $A = 0$ ,  $B = 1$  then  $A$  and  $B$  inputs of second NOR gate will be 0 and hence  $Y = 1$ . Similarly work out the values of  $Y$  for other combinations of  $A$  and  $B$ . Compare with the truth table of OR, AND, NOT gates and find the correct one.)

**Solution:** The inputs of the given circuit are  $A$  and  $B$ . The first NOR gate has as its input  $\overline{A+B}$ . The inputs of the second NOR gate become the outputs of the first.

Hence, the output of combination is:

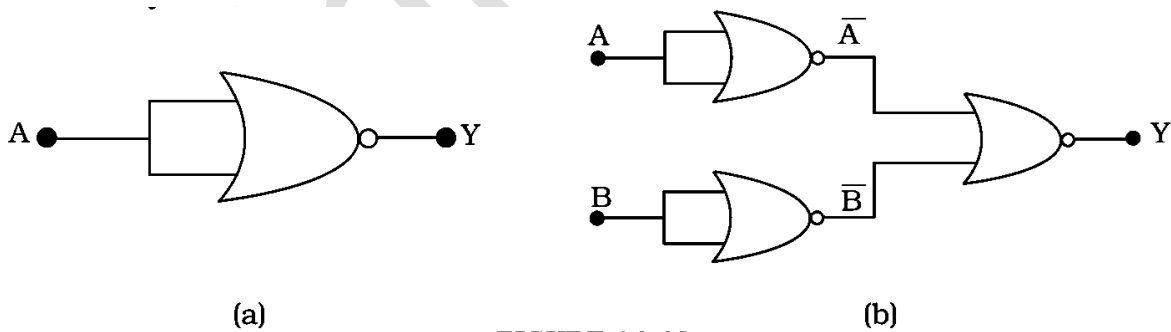
$$\begin{aligned}
 Y &= \overline{\overline{A+B} + \overline{A+B}} \\
 &= \overline{\overline{A+B}} \\
 &= \overline{\overline{A+B}} \\
 &= \overline{\overline{A+B}} \\
 &= A+B
 \end{aligned}$$

The truth table for this operation is:

$A$	$B$	$Y(= A+B)$
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table of an OR gate. Hence this circuit functions as an OR gate.

**Question 14.19:** Write the truth table for the circuits given in Fig. 14.40 consisting of NOR gates only. Identify the logic operations (OR, AND, NOR) performed by the two circuits.



**FIGURE 14.40**

**Solution:** (a) The NOR gate's inputs are  $A$ , and the output is  $Y$ . As a result, the circuit's output is  $\overline{A+A}$

Output,  $Y = \overline{A+A} = \overline{A}$

The truth table is given as:

$A$	$Y = \overline{A}$

0	1
1	0

This is the truth table of a NOT gate. Hence this circuit functions as a NOT gate.

(b) The given circuit's inputs are A and B, and the output is Y. Using the result obtained in solution (a), we may deduce that the first two NOR gates' outputs are  $\overline{A}$  and  $\overline{B}$ , are the inputs for the last NOR gate. Hence the output for the circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

The truth table for same can be written as :

A	B	$Y = A/B$
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table of an AND gate. Hence this circuit functions as an AND gate.